**WHAT IS CLAIMED IS:**

1. A flash memory cell, comprising:

a tunnel oxide film formed at a given region of a SOI substrate;

a floating gate on the tunnel oxide film;

a dielectric film on the floating gate;

first and second channel regions at the SOI substrate below both ends of the floating gate;

a source region formed between the first and second channel regions;

first and second drain regions at the SOI substrate at both sides of the floating gate; and

a word line formed on the dielectric film,

wherein data of two bits or four bits are stored at a single cell by individually injecting electrons into the floating gate on the first and second channel regions or discharging the injected electrons, depending on voltages applied to the source region, the word line, and the first and second drain regions.

2. The flash memory cell as Claimed in claim 1, wherein said floating gate is consisting of a nitride film.

3. The flash memory cell as Claimed in claim 1, wherein the first and second channel regions each consist of a P type impurity region and wherein the first and second drain regions consist of a N type impurity region.

4. The flash memory cell as Claimed in claim 3, wherein the first and second drain regions are formed in a P type impurity region forming the first channel region and a P type impurity region forming the second channel region, respectively.

5. The flash memory cell as Claimed in claim 1, wherein a lower portion of the source region is precluded from an insulating film included in the SOI substrate, by which the source region is electrically isolated from other source regions.

6. The flash memory cell as Claimed in claim 1, further comprising a device isolation film formed on the first and second drain regions, wherein the floating gate is separated by the device isolation film.

7. The flash memory cell as Claimed in claim 1, further comprising a contact plug formed to be electrically connected with the source region, and the first and second drain regions.

8. The flash memory cell as Claimed in claim 7, wherein said contact plug is included one by one every 5 through 10 cells and the number of the contact plug is controlled by a design rule or a voltage to be applied.

9. A method of manufacturing a flash memory cell, comprising the steps

of:

forming a P type impurity region and a source region at a SOI substrate;

forming a drain region consisting of an N type impurity region at the central region of the P type impurity region;

forming a device isolation film on the drain region;

forming a stack structure in which a tunnel oxide film, a floating gate and a dielectric film are stacked on the source region and the P type impurity region, wherein the stack structure are separated by the device isolation film and both ends of the stack structure are overlapped with a portion of the P type impurity region; and

forming a conductive material layer and then forming a word line by means of an etching process using a word line mask.

10. The method as claimed in Claim 9, wherein said SOI substrate has a stack structure in which a silicon substrate, a insulating layer and a silicon layer doped N type impurities are sequentially formed, said source region consists of the silicon layer.

11. The method as claimed in Claim 9, wherein said floating gate consists of a nitride film, said dielectric film consists of an oxide film, and said tunnel oxide film, said floating gate and said dielectric film have an ONO structure.

12. The method as claimed in Claim 9, further comprising the step of, after

the etching process for the word line is performed, etching said dielectric film, said floating gate and said tunnel oxide film by means of a self-aligned etching process.

13. The method as claimed in Claim 9, further comprising the step of, after said interlayer insulating film is formed on the entire structure, forming a contact plug connected with a given region of said source region and said drain region.

14. The method as claimed in Claim 13, wherein said contact plug is formed one by one every 5 through 10 cells and the number of the contact plug is varied depending on a design rule or a voltage to be applied.

15. A method of manufacturing a flash memory cell, comprising the steps of:

forming a P type impurity region and a source region at a SOI substrate;

forming a drain region consisting of an N type impurity region at the central region of the P type impurity region;

forming a device isolation film at the drain region, and a tunnel oxide film at the P type impurity region and the source region, by means of a thermal oxidization process;

forming a floating gate and a dielectric film having a stack structure on the tunnel oxide film; and

forming a conductive material layer and then forming a word line by means of an etching process using a word line mask.

16. The method as claimed in Claim 15, wherein said SOI substrate has a stack structure in which a silicon substrate, a insulating layer and a silicon layer doped N type impurities are sequentially formed, said source region consists of the silicon layer.

17. The method as claimed in Claim 15, wherein said floating gate consists of a nitride film, said dielectric film consists of an oxide film, and said tunnel oxide film, said floating gate and said dielectric film have an ONO structure.

18. The method as claimed in Claim 15, further comprising the step of, after the etching process for the word line is performed, etching said dielectric film, said floating gate and said tunnel oxide film by means of a self-aligned etching process.

19. The method as claimed in Claim 15, further comprising the step of, after said interlayer insulating film is formed on the entire structure, forming a contact plug connected with a given region of said source region and said drain region.

20. The method as claimed in Claim 19, wherein said contact plug is formed one by one every 5 through 10 cells and the number of the contact plug

is varied depending on a design rule or a voltage to be applied.

21. A method of programming a flash memory cell for storing data at the flash memory cell claimed in Claim 1 is characterized in that:

in a state that the word line is applied with a program voltage and the source region is connected to a ground terminal,

the second drain region is connected to the ground terminal and the first drain region is applied with a voltage of about 5V, in case that the electrons are injected into one end of the floating gate consisting of a nitride film; and

the first drain region is connected to the ground terminal and the second drain region is applied with a voltage of about 5V, in case that electrons are injected into the other end of the floating gate,

whereby electrons are independently injected into one end and the other end of the floating gate to store data of two bits at a single cell.

22. The method as claimed in any of Claim 21, wherein said program voltage is 9V through 10V.

23. The method as claimed in any of Claim 21, wherein all the regions of other cells are floated in the process of injecting electrons into the floating gate.

24. A method of programming a flash memory cell for storing data at the flash memory cell claimed in Claim 1 is characterized in that:

in a state that the word line is applied with a program voltage and the source region is applied with a voltage of about 5V,

the first drain region is connected to the ground terminal and the second drain region is floated, in case that the electrons are injected into one end of the floating gate consisting of a nitride film; and

the second drain region is connected to the ground terminal and the first drain region is floated, in case that electrons are injected into the other end of the floating gate,

whereby electrons are independently injected into one end and the other end of the floating gate to store data of two bits at a single cell.

25. The method as claimed in any of Claim 24, wherein said program voltage is 9V through 10V.

26. The method as claimed in any of Claim 24, wherein all the regions of other cells are floated in the process of injecting electrons into the floating gate.

27. A method of programming a flash memory cell for storing data at the flash memory cell claimed in Claim 1 is characterized in that:

one end of the floating gate is programmed with four states, by selectively performing: a first programming operation by which electrons are into a left side of one end of the floating gate by connecting the source region to the ground terminal and applying a voltage of about 5V to the first drain region, in a state that the word line is applied with a program voltage and the

second drain region is connected to the ground terminal; and a second programming operation by which electrons are injected into a right side of one end of the floating gate by applying a voltage of about 5V to the source region and connecting the first drain region to the ground terminal, in a state that the word line is applied with a program voltage and the second drain region is floated, and

the other end of the floating gate is programmed by the same method, whereby data of four bits are stored at a single flash memory cell.

28. The method as claimed in Claim 27, wherein said four states includes:

a first state that electrons are not injected into one end of the floating gate,

a second state that electrons are injected only into a left side of one side of the floating gate,

a third state that electrons are injected only into a right side of one side of the floating gate, and

a fourth state that electrons are injected into the entire one end of the floating gate.

29. The method as claimed in any of Claim 27, wherein said program voltage is 9V through 10V.

30. The method as claimed in any of Claim 27, wherein all the regions of other cells are floated in the process of injecting electrons into the floating gate.

31. A method of erasing a flash memory cell for erasing data stored at the flash memory cell claimed in Claim 1 is characterized in that: in a state that the word line is applied with an erase voltage and the source region is floated, a voltage of 5V is applied to the first and second drain regions to discharge electrons injected into one end and the other end of the floating gate consisting of a nitride film, thus performing an erase operation.

32. The method as claimed in Claim 31, wherein said erase voltage is -10V through -12V.

33. The method as claimed in Claim 31, wherein all the regions of other cells are floated in the process of discharging electrons injected into the floating gate.

34. A method of reading a flash memory cell for reading data stored at the flash memory cell claimed in Claim 1 is characterized in that: in a state that the word line is applied with a read voltage and the source region is applied with a voltage of 0 through 0.8V, the first and second cell currents flowing into the first and second channel regions are sensed to determine a programming state of one end and the other end of the floating gate, thus reading data of two bits stored at the flash memory cell.

35. The method as claimed in Claim 34, wherein said read voltage is about

3V.

36. The method as claimed in any of Claims 34, wherein the first and second cell currents of the first and second drain regions are sensed by connecting a current mirror to the first and second drain regions.

37. A method of reading a flash memory cell for reading data stored at the flash memory cell claimed in Claim 27 for which the programming operation is performed is characterized in that:

the first drain region is connected to the ground terminal and the first cell current flowing into the source region is then sensed, in a state that the word line is applied with a read voltage and the source region is applied with a voltage of about 1V, and the source region is connected to the ground terminal and the second cell current flowing into the first drain region is then sensed, in a state that the word line is applied with a read voltage and the first drain region is applied with a voltage of about 1V, whereby data of two bits stored at one end of the floating gate are detected; and

data of four bits stored at the flash memory cell are read by sensing the current flowing into the other end of the floating gate using the same method.

38. The method as claimed in any of Claims 37, wherein said read voltage is about 3V.

39. The method as claimed in any of Claims 37, wherein the second drain

region is floated in the process of sensing the first and second currents.

40. The method as claimed in any of Claims 37, wherein said data of the two bits are discriminated as:

'11' corresponding to a case that both the first and second currents are sensed to have a given value,

'10' corresponding to a case that the first current is sensed to have a given value and the second current is sensed to have 0A,

'01' corresponding to a case that the first current is sensed to have 0A and the second current is sensed to have a given value, and

'00' corresponding to a case that both the first and second currents are sensed to have 0A.